BHARATI VIDYAPEETH
(DEEMED TO BE UNIVERSITY)
COLLEGE OF ENGINEERING, PUNE – 411043
Electronics Engineering Department

Class Time Table (TERM -II A.Y. 2018-19)

CLASS: **B.Tech. (Electronics) SEM: VI** CLASS ROOM NO: W-404B (w.e.f. 02/01/2019)
GFM : Mr.-S.R. MADKAR

TIME	MON	TUE	WED	THU	FRI	TIME	SAT
9:15	DSP-A-W-302-SRM; ES-B-W304-PAC; VLSID-C-W305-ARP; ECD-D-W-402-SVD.	PM & F SRM	DSP-C-W-302-MVP; ES-D-W304-PAC; VLSID-E-W305-MSC; ECD-F-W-402-SRM.	DSP-D-W-302-MVP; ES-E-W304-PAC; VLSID-F-W305-ARP; ECD-A-W-402-SRM.	VLSID ARP	**8.30**	ES PAC
10:15		ECD AAS			ECD AAS	**9.30**	DSP MVP
11.15	**R E C E S S**					**10.30**	Staff Meeting
11:30	DSP MVP	DSP-B-W-302-MVP; ES-C-W304-PRN; VLSID-D-W305-ARP; ECD-E-W-402-SRM.	ECD AAS	PM & F SRM	DSP-E-W-302-MVP; ES-F-W304-PAC; VLSID-A-W305-ARP; ECD-B-W-402-SRM.	**11:30**	DSP-F-W-302-SRM; ES-A-W304-PRN; VLSID-B-W305-ARP; ECD-C-W-402-SVD.
12:30	ECD AAS		DSP MVP	VLSID ARP		**12:30**	
1:30	**R E C E S S**						
2:15	VLSID ARP	**PSD -VI**	**PSD -VI**	DSP MVP	ES PAC		
3:15	**NS**	**PSD -VI**	**PSD -VI**	ES PAC	PM & F SRM		

Faculty Name	Subject	L	T	P	Total
M. V. PATIL	DSP-Digital Signal Processing	04	-	08	12
S. R. MADKAR	DSP-Digital Signal Processing	-		04	04
P. A. CHOUGULE	ES-Embedded System	03	-	08	11
P. R. NAREGALKAR	ES-Embedded System	-		04	04
A.R.PATIL	VLSID-VLSI Design	03	-	10	13
M.S.CHAVAN	VLSID-VLSI Design	-		02	02
S. R. MADKAR	PM&F-Project Management & Finance	03	-	-	03
A. A. SHINDE	ECD-Electronic Circuit Design	04	-	-	04
S. R. MADKAR	ECD-Electronic Circuit Design	00	-	08	12
S.V.DHOLE	ECD-Electronic Circuit Design	-	-	04	04
VISITING FACULTY	PSD-VI Professional Skill Development-VI	04	-	-	04
	Total	21	00	36	57