BHARATI VIDYAPEETH (DEEMED TO BE UNIVERSITY)
COLLEGE OF ENGINEERING
DHANKAWADI, PUNE – 411043
Electronics Engineering Department

Class Time Table(TERM -II A.Y. 2019-20)

CLASS: B.Tech. (ELECTRONICS) SEM:VI CLASS ROOM NO: W404B

(w.e.f. 01/ 01/ 2020)

GFM : Mrs M. V. Patil (Mobile - 9226418220)

TIME	MON	TUE	WED	THU	FRI	TIME	SAT
09:15	DSP-A-W302-SRM; ES-B-W304 PAC; VLSID-C W305-MSC; ECD-D-W-402 NTM.	PM & F SRM	DSP-C-W-302-MVP; ES-D-W304-PRN; VLSID-E-W305-MSC; ECD-F-W-402-SRM.	DSP MVP	VLSID ARP	8.30	DSP-F-W302-SKP; ES-A-W304-PAC; VLSID-B-W305-ARP; ECD-C-W402-SVD.
10:15		ECD AAS		VLSID ARP	ECD NTM	9.30	
11:15	**REC E SS**					10:30	STAFF MEETING
11:30	ECD NTM	DSP-B-W-302-MVP; ES-C-W304 PAC; VLSID-DW305 ARP; ECD-E-W-402 SVD.	ECD AAS	DSP-D-W-302-SRM; ES-E-W304-PAC; VLSID-F-W305-ARP; ECD-A-W-402-NTM	ES PAC	11:30	ES PAC
12:30	ES PAC		DSP MVP		DSP MVP	12:30	PM & F SRM
1:30	R E C E S S						
02:15	VLSID ARP	**PSD -VI**	**PSD -VI**	PM & F SRM	DSP-E-W-302-MVP; ES-F-W304-PAC; VLSID-A-W305-ARP; ECD-B-W402-SRM.	.	
03:15	DSP MVP	**PSD -VI**	**PSD -VI**	**NS**			

Faculty Name	Subject	L	T	P	Total
M. V. PATIL	DSP-Digital Signal Processing	04	-	06	10
S. R. MADKAR	DSP-Digital Signal Processing	-	-	04	04
S.K.PAWAR	DSP-Digital Signal Processing	-	-	02	02
P. A. CHOUGULE	ES-Embedded System	03	-	10	13
P. R. NAREGALKAR	ES-Embedded System	-		02	02
A.R.PATIL	VLSID-VLSI Design	03	-	10	13
M.S.CHAVAN	VLSID-VLSI Design	-		04	04
S. R. MADKAR	PM&F-Project Management & Finance	03	-	-	03
A. A. SHINDE	ECD-Electronic Circuit Design	02	-	-	02
N.T.MADKAD	ECD-Electronic Circuit Design	02	-	-	02
S. R. MADKAR	ECD-Electronic Circuit Design	-	-	04	04
S.V.DHOLE	ECD-Electronic Circuit Design	-	-	04	04
VISITING FACULTY	PSD-VI Professional Skill Development-VI	04	-	-	04
	Total	21	00	42	63